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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/751,610	12/29/2000	William A. Harris	H16-26054 US	8597

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EXAMINER
COX, CASSANDRA F

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 11/27/2001

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/751,610	HARRIS, WILLIAM A.	
	Examiner	Art Unit	
	Cassandra Cox	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 December 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 December 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4*
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Drawings

1. The drawings are objected to because in Figure 2 there is no connection between output 217 and the clock input (CLK) of flip-flop 220. Correction is required.

Claim Objections

1. Claims 7 and 16 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Claim 7 is not further limiting because applicant has already claimed the subject matter of the claim in lines 5-6 of claim 6. Claim 16 is not further limiting because applicant has already claimed the subject matter of the claims in lines 4-5 of claim 13.

2. Claim 1 is objected to because of the following informalities: In line 2 of claim 1, the phrase "clock signals" should be deleted. Appropriate correction is required.

3. Claim 20 is objected to because of the following informalities: In line 9 of claim 20, the word "shift" should be replaced with the word --lock--. Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, and 4-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Li et al. (U.S. Patent No. 5,058,132).

In reference to claim 1, Li discloses in Figure 2, a circuit (100) for dividing an input clock signal (116) into N clock signals having a relative phase separation of 360°/2N, where N is a positive integer, the circuit comprising: a phase lock loop circuit (102) receiving an input signal (116) having a frequency F_0 and providing an out put signal having a frequency $2NF_0$; and a Johnson counter (114) having N stages connected to receive as an input the output signal (124) of the phase lock loop circuit (102) and providing an output signal(LBC1-5) as an error signal to the phase lock loop circuit (column 5, lines 25-28); the Johnson counter (114) also connected for providing at least two output signals (LBC1-LBC5) from at least two of the N stages of the Johnson counter (114) as clock signals each having a phase displaced from the phase of the other 360°/2N (which is seen to be an inherent function of the Johnson counter). The same applies to claims 4-5, 11-12, and 20, wherein the multistage counting circuit is seen to be the Johnson counter (114) and the clock generator is seen to be the oscillator (120; column 4, line 65 - column 5, line 15).

In reference to claim 6, Li discloses in Figure 2, a circuit for receiving an input clock signal (116) and generating a plurality of clock signals (LBC1-LBC5) having frequencies identical to the input clock signal (116) and predetermined phase displacements from the input signal, comprising: a phase detector (104) for comparing

an input clock signal (116) to a feedback signal (123) and providing an output signal (121) corresponding to the phase difference between the input clock signal (116) and the feedback signal (123); a low pass filter and gain stage (106) receiving the output signal from the phase comparator (104) and producing a control signal (125); a voltage controlled oscillator (108) for receiving the control signal and producing an oscillator output signal (124) having a frequency corresponding to the control signal (125); and a multistage counting circuit (114) connected to receive the oscillator output signal (124) and provide the feedback signal (123; column 5, lines 50-67) to the phase detector (104) and a plurality of clock signals (LBC1-LBC5) at the frequency of the input clock signal (116) and phase shifted from the clock signal by fixed angular increments. The same applies to claims 7, 13-14, and 16.

In reference to claim 8, Li also discloses in column 5, lines 1-22 that the frequency (125MHz) of the voltage controlled oscillator output signal (124) is a multiple of the frequency (12.5 MHz) of the input clock signal (116). The same applies to claims 10, 17, and 19.

In reference to claim 9, Li also discloses in Figure 2 that the multistage counting circuit (114) is a Johnson counter having N stages. The same applies to claims 15 and 18.

6. Claims 1 and 4-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Fujii (U.S. Patent No. 5,315,269).

In reference to claim 1, Fujii discloses in Figure 5, a circuit for dividing an input clock signal (which is seen as the output of the first frequency demultiplier, 104) into N

clock signals having a relative phase separation of 360°/2N, where N is a positive integer, the circuit comprising: a phase lock loop circuit (101, 102, 103) receiving an input signal having a frequency F_0 and providing an output signal having a frequency $2NF_0$; and a Johnson counter (105; see column 5, lines 1-2 and 14-16) having N stages connected to receive as an input the output signal (OUT) of the phase lock loop circuit (101, 102, 103) and providing an output signal as an error signal to the phase lock loop circuit (column 3, lines 60-63); the Johnson counter (105) also connected for providing at least two output signals (shown in Figure 8) from at least two of the N stages of the Johnson counter (105) as clock signals each having a phase displaced from the phase of the other by 360°/2N (which is seen to be an inherent function of the Johnson counter). The same applies to claims 4-5, 11-12, and 20, wherein the multistage counting circuit is seen to be the Johnson counter (105 shown in Figure 8, see column 5, lines 1-16) and the clock generator is seen to be the first frequency demultiplier (104).

In reference to claim 6, Fujii discloses in Figure 7, a circuit for receiving an input clock signal (61-64) and generating a plurality of clock signals (71-74) having frequencies identical to the input clock signal (61-64) and predetermined phase displacements from the input signal, comprising: a phase detector (11-14) for comparing an input clock signal (61-64) to a feedback signal (71-74) and providing an output signal (OUT) corresponding to the phase difference between the input clock signal (61-64) and the feedback signal (71-74); a low pass filter and gain stage (102) receiving the output signal from the phase comparator (11-14) and producing a control signal; a voltage controlled oscillator (VCO) for receiving the control signal and producing an oscillator

output signal (OUT) having a frequency corresponding to the control signal; and a multistage counting circuit (105, shown in Figure 8) connected to receive the oscillator output signal (OUT) and provide the feedback signal (71-74) to the phase detector (11-14) and a plurality of clock signals (71-74) at the frequency of the input clock signal (61-64) and phase shifted from the clock signal by fixed angular increments. The same applies to claims 7, 13-14, and 16.

In reference to claim 8, Fujii also discloses in column 4, lines 3-8 that the frequency ($\pm 2N\pi$) of the voltage controlled oscillator output signal (OUT) is a multiple of the frequency ($\pm 2\pi$) of the input clock signal (116). The same applies to claims 10, 17, and 19.

In reference to claim 9, Fujii also discloses in Figure 8, column 5, lines 1-16 that the multistage counting circuit (105) is a Johnson counter having N stages. The same applies to claims 15 and 18.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 2-3 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujii (U.S. Patent No. 5,315,269).

In reference to claim 2, Fujii discloses all of the limitations of the claim as mentioned above with reference to claim 1, except that Fujii does not disclose that N is equal to 4. Fujii does say, however, that N is a predetermined number (column 4, lines 1-3). Therefore, it would have been obvious to one of ordinary skill in the art that the value of N could be any number including 4, dependent on the particular environment and the desired results of the circuit. The same applies to claims 3 and 21.

9. Claims 2-3, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Li (U.S. Patent No. 5,058,132) in view of Fujii (U.S. Patent No. 5,315,269).

Li discloses all of the limitations of claim 2, as mentioned above with reference to claim 1, except that N is 4 (wherein N is seen as the number of stages in the Johnson counter, 114). Fujii discloses a circuit in Figure 5 wherein the value of N could be any number (column 4, lines 1-3). It would have been obvious to one having ordinary skill in the art that the Johnson counter (105) of Fujii could be used in place of the Johnson counter (114) in the circuit of Li, for the advantage of being able to change the divider ratio of the output signal. The same applies to claims 3 and 21.

Double Patenting

10. Applicant is advised that should claim 8 be found allowable, claim 10 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing

one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

11. Applicant is advised that should claim 15 be found allowable, claim 18 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Takahashi et al. (U.S. Patent No. 5,847,570) and Tanaka (U.S. Patent No. 5,479,458) both disclose circuits having phase lock loops and Johnson counters.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cassandra Cox whose telephone number is 703-306-5735. The examiner can normally be reached on Monday-Thursday from 7:00 AM to 4:30 PM and on alternate Fridays from 7:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (703)-308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are 703-

308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

CC

November 9, 2001

Kenneth B. Wells
Primary Examiner